

CLAIMS

I Claim:

Sub A1
1. An inverter circuit connected to a load and having a pair of switching transistors, each having a base-emitter junction, and adapted to convert DC voltage supplied from a DC source having positive and negative terminals into an AC output voltage comprising:

first drive circuit means connected between the base-emitter junctions of the transistors and operable to provide intermittent positive feedback signals for causing the alternating conduction of the transistors; and

second drive circuit means also connected between the base-emitter junctions of the transistors and operable to provide intermittent subtractive feedback signals for rapidly turning off a conducting transistor whereby an alternating current is caused to flow through the load.

2. The inverter circuit of Claim 1 wherein:

said first drive circuit means includes a saturable current transformer with a magnetic core.

3. The inverter circuit of Claim 2 wherein:

said current transformer is effective to deliver a positive feedback signal until such time as said core becomes saturated.

4. The inverter circuit of Claim 1 wherein:

said second drive circuit means includes a non-saturable current transformer.

5. The inverter circuit of Claim 4 wherein:

said non-saturable transformer delivers said subtractive feedback signal after said core of said first drive circuit means becomes saturated.

6. The inverter circuit of Claim 5 wherein:

said first current transformer is connected to the base-emitter junction of each of said transistors, and

said second current transformer is also connected to a base-emitter junction of each of said transistors.

7. The inverter circuit of Claim 5 including:

a power output transformer having a winding with a center-tap connected to the positive terminal of the DC source; and

said second current transformer has a winding with a center-tap connected to the negative terminal of the DC source.

8. The inverter circuit of Claim 1 wherein:

said circuit is self-oscillating for controlling the conduction of the switching transistors.

9. The inverter circuit of Claim 1 wherein:

each of the switching transistors has a collector element; and

a capacitor is connected between said collector elements.

10. The inverter circuit of Claim 1 including:

a power output transformer with some shunt leakage inductance also connected to the collectors of the transistors.

11. An inverter circuit connected to a load and having a pair of switching transistors connected in series across a source of DC voltage, with each transistor having a base-emitter junction, and adapted to convert DC voltage supplied from the DC source into an AC output voltage comprising:

first drive circuit means connected between the base-emitter junction of the transistors and operable to provide intermittent positive feedback signal for causing the alternating conduction of the transistors; and

second drive circuit means also connected between the base-emitter junction of the transistors and operable to provide intermittent subtractive feedback signals for rapidly turning off a conducting transistor whereby an alternating current is caused to flow through the load.

Sub A2

12. The inverter circuit of Claim 11 including:

a voltage divider connected across said DC source and operable to provide a divided DC voltage to said drive circuit means.

13. The inverter circuit of Claim 12 wherein:

said voltage divider is a series connection of at least two capacitors.

14. *Sub A2* The inverter circuit of Claim 12 including:

a power output transformer connected between the transistors and said voltage divider and operable to deliver an AC output voltage produced by the alternating conduction of the transistors to the load.

15. An electrical inverter circuit having a pair of alternately conducting switching transistors, each with a collector and base-emitter junction and adapted to convert a unidirectional input voltage into an alternating output voltage comprising:

drive control means effective to provide subtractive bias means to the base-emitter junctions of both transistors during periods when their collector-emitter voltages are significantly greater than the transistor collector-emitter saturation voltages.

16. The inverter circuit of Claim 15 including:

an output transformer having significant shunt leakage inductance connected to the collectors of the transistors and effective to produce large voltage swings at the collectors of the transistors.

17. The inverter circuit of Claim 16 including:

a capacitor effectively connected in parallel with said transformer and effective to limit the rate of voltage rise and decline at the collectors of the transistors.

18. The inverter circuit of Claim 17 wherein:

said drive control means includes positive feedback means whereby the inverter circuit is self-oscillating.

19. The inverter circuit of Claim 18 wherein:

said positive feedback means includes a saturable transformer connected between said output transformer and the base-emitter junctions of the transistors.

20. The inverter circuit of Claim 19 wherein:

said saturable transformer is a current transformer.

21. *Sub A3* The inverter circuit of Claim 15 wherein:

said subtractive bias means includes a non-saturable current transformer.

22. An electrical inverter circuit containing a pair of alternately conducting switching transistors, each having a collector, base and emitter, and adapted to convert a uni-directional input voltage into an alternating output voltage, and with each transistor having a cyclical emitter-collector voltage waveform characterized by four distinct periods within each cycle, namely: a period when the magnitude is low and sub-

stantially constant, a period when it increases rapidly, a period when it is high and substantially constant, and a period when it decreases rapidly and including:

drive control means connected to the base-emitter junction of each transistor and operable to maintain each reversely biased during all periods other than the period when its voltage is low and substantially constant.

23. The inverter circuit of Claim 22 wherein:

said drive control means biases the base-emitter junction forwardly during the period when its voltage is low and substantially constant.

24. An electrical inverter circuit containing a pair of alternately conducting switching transistors, each having a base-emitter junction and a collector-emitter junction, and adapted to convert a unidirectional input voltage into an alternating output voltage, comprising:

reverse bias means connected to the base-emitter junction of each transistor and operable to maintain each transistor reversely biased whenever its collector-emitter voltage is substantially greater than its collector-emitter saturation voltage.

25. An electrical inverter circuit containing a pair of alternately conducting switching transistors, each having a collector and base-emitter junction, and adapted to convert a unidirectional input voltage into a cyclical, trapezoidal shaped, alternating output voltage comprising:

control means connected to said transistors and operable to effect alternating periodic conduction thereof, said control

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means supplying to the base-emitter junction of each transistor
q a control signal effective to turn on a transistor only after
its collector voltage has dropped substantially to its lowest
ll level.

26. The electrical inverter circuit of Claim 25 wherein:

said control means is operable to turn off a transistor
by reversing the control signal supplied to said base-emitter
junction.

27. The electrical inverter circuit of Claim 26 wherein:

said base-emitter junction has stored charge carriers
while conducting, and

said control means is effective to turn off a transistor
by the forced evacuation of charge carriers from said base-emitter
junction.

28. The inverter circuit of Claim 25 wherein:

said drive control means includes a current feedback
transformer having at least one primary winding and a secondary
winding for supplying said control signals.

29. The inverter circuit of Claim 28 including:

a power output transformer having some shunt leakage
inductance for delivering the alternating output voltage;

a capacitor connected between the collectors of the
transistors; and

said current feedback transformer primary winding
being connected between said output transformer and said
capacitor.

Sub Q5

30. The inverter circuit of Claim 29 wherein:

said output transformer stores sufficient inductive energy in its leakage inductance to cause the voltage at the collector of a first non-conducting transistor to rise to a level twice the magnitude of the unidirectional input voltage.

Sub Q5

31. *Q5* The inverter circuit of Claim 25 wherein:

Sub Q5

said control means is self-oscillating.

32. The inverter circuit of Claim 25 including:

a shunting diode connected across the base-emitter junction of each transistor.

Sub Q6

33. *Q6* The inverter circuit of Claim 32 wherein:

Sub Q6

a first diode shunting the base-emitter junction of a first transistor is operable to function as a clamp so as to limit the voltage rise at the collector of said first transistor to twice the magnitude of the unidirectional input voltage.

34. The inverter of Claim 33 including:

a shunting diode connected across the collector-emitter terminals of each transistor.

35. A push-pull electrical inverter circuit having a pair of alternately conducting switching transistors, each having a control input element, and adapted to convert a unidirectional input voltage into an alternating output

voltage comprising:

first drive control means including saturable

- 7 current feedback means for supplying positively conducting control signals to the control input element of each transistor; and

second drive control means including non-saturable

- 11 current feedback means for supplying subtractive control signals to the control input element of each transistor after said first saturable feedback means has saturated whereby a conducting transistor is rapidly and efficiently turned off.

36. An electrical inverter circuit having a pair of switching transistors, each with a control input element, and adapted to convert a unidirectional input voltage supplied from a source having a pair of input terminals into an alternating output voltage comprising:

a series connection of the two transistors between the input terminals;

first saturable feedback means connected to the control

- 4 input elements of the transistors for supplying positive control signals; and

second non-saturable feedback means also connected to the control input elements of the transistors for supplying

- 15 subtractive control signals for alternately turning off a transistor.

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